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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,020	CLEMENTI ET AL.	
	Examiner	Art Unit	
	Eric B. Chen	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☒ Claim(s) *13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/6/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Objections

2. Claim 13 objected to because of the following informalities: "an isotropic" apparently should be -- anisotropic --. Otherwise, claim 13 would be inconsistent with the Specification. Appropriate correction is required.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

4. A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory

double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

5. Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. Claims 1, 3, 15-18, and 22-26 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-2 and 7-15 of copending Application No. 10/746,878, Clementi et al., in view of Kerber et al. (U.S. Patent No. 6,027,972).

7. As to claim 1, Clementi claims a method for manufacturing non-volatile memory cells on a semiconductive substrate (claim 1, page 15, lines 1-2), comprising at least the following steps: forming active areas in said semiconductive substrate, bounded by portions of an insulating layer (claim 1, page 15, lines 3-4); forming a first thin layer of tunnel oxide and depositing a first layer of conductive material on said active areas (claim 1, page 15, lines 5-6); defining a plurality of floating gate regions, wherein the definition of the floating gate regions comprises the steps of (claim 1, page 15, lines 7-8): forming a plurality of alternated stripes of a first material above active areas alternated by active areas lacking stripes (claim 1, page 15, lines 9-10); forming spacers of a second material in the shelter of the side walls of said stripes, said second material being selectively etchable with respect to said first material (claim 1, page 15, line 11), depositing a layer of a third material in order to fill in the space between said spacers (claim 1, page 15, lines 12-13), planarizing said layer of a

third material together with said alternated stripes and said spacers (claim 1, page 15, lines 14-15) and; selectively removing said spacers in order to expose portions of said first layer of semiconductive material (claim 1, page 15, line 16).

8. Clementi does not expressly claim etching said first layer of semiconductive material in order to form grooves in correspondence with its exposed portions; and selectively removing said alternated stripes and said layer of a third material. Kerber discloses a method for manufacturing non-volatile memory cells on a semiconductive substrate, including the steps of etching said first layer of semiconductive material (80) in order to form grooves in correspondence of its exposed portions (column 6, lines 38-41; Figure 2C), selectively removing said alternating stripes (60) (column 6, lines 35-36) and said layer of a third material (80) (column 6, lines 42-43). Kerber's method is directed to producing small structural widths in transistors (column 6, lines 8-11), including etching features to complete the electrical device (column 6, lines 35-64). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the steps of etching said first layer of semiconductive material in order to form grooves in correspondence of its exposed portions, selectively removing said alternating stripes and said layer of a third material. One who is skilled in the art would be motivated to include etching steps to complete the fabrication of the device.

9. As to claim 3, Clementi claims that said plurality of alternated stripes is formed by depositing a second layer of conductive material and by defining said

second layer of conductive material by means of lithography (claim 2, page 15, lines 1-3).

10. As to claim 15, Clementi claims a semiconductor fabrication method, comprising: forming a plurality of first stripes which lie above first alternating active areas (claim 7, page 18, line 2); forming sidewall spacers for the plurality of first stripes (claim 7, page 18, line 3); forming a plurality of second stripes between the sidewall spacers over the insulated base polysilicon layer which lie above second alternating active areas (claim 7, page 18, lines 4-5); and removing the sidewall spacers (claim 7, page 18, line 6).

11. Clementi does not expressly disclose an insulated base polysilicon layer. Kerber teaches that an insulated base polysilicon layer (50) (column 6, lines 23-28) is conventional structure in memory cells (column 6, lines 12-15). Therefore, it would have been obvious to one of ordinary skill in the art to form a plurality of first stripes over an insulated base polysilicon layer. One who is skilled in the art would be motivated to use a conventional structure in forming a memory device.

12. As to claim 16, Clementi claims that forming the plurality of first stripes comprises: depositing a first material layer (claim 8, page 18, line 3); defining the first stripes in the first material layer using a photolithography mask (claim 8, page 18, lines 4-5); etching using the mask to remove the first material layer but leave the first stripes (claim 8, page 18, lines 6-7).

13. As to claim 17, Clementi claims that forming the plurality of second stripes comprises: depositing a second material layer that covers the first stripes and fills a region between sidewall spacers (claim 9, page 18, lines 3-4); planarizing to

remove the second material layer but leave the second stripes (claim 9, page 18, lines 5-6).

14. As to claim 18, Clementi claims that forming sidewall spacers comprises: depositing a nitride layer (claim 10, page 19, line 2); and patterning the nitride layer to remove the nitride layer above the second alternating active areas but leave the nitride layer adjacent sidewalls of the first stripes (claim 10, page 19, lines 3-4).

15. As to claim 22, Clementi claims a method for semiconductor fabrication on a substrate including a plurality of active areas (claim 11, page 20, lines 1-2), comprising: forming a plurality of first stripes by photolithographic techniques which lie above even ones of the plurality of active areas (claim 11, page 20, lines 3-4); and forming a plurality of second stripes without the use of photolithographic techniques over the insulated base polysilicon layer and which lie above odd ones of the plurality of active areas (claim 11, page 20, lines 5-6).

16. Clementi does not expressly disclose an insulated base polysilicon layer. Kerber teaches that an insulated base polysilicon layer (50) (column 6, lines 23-28) is conventional structure in memory cells (column 6, lines 12-15). Therefore, it would have been obvious to one of ordinary skill in the art to form a plurality of first stripes over an insulated base polysilicon layer. One who is skilled in the art would be motivated to use a conventional structure in forming a memory device.

17. As to claim 23, Clementi claims forming a plurality of first stripes (claim 12, page 20, line 1) comprises: depositing a first material layer (claim 12, page 20, line 3); defining the first stripes in the first material layer using a photolithography

mask (claim 12, page 20, lines 4-5); etching using the mask to remove the first material layer but leave the first stripes (claim 12, page 20, lines 6-7).

18. As to claim 24, Clementi claims forming the plurality of second stripes (claim 13, page 20, lines 1-2) comprises: forming sidewall spacers for the plurality of first stripes (claim 13, page 20, line 3); forming the plurality of second stripes between the sidewall spacers over odd ones of the active areas (claim 13, page 20, lines 4-5); and removing the sidewall spacers (claim 13, page 20, line 6).

19. As to claim 25, Clementi claims forming the plurality of second stripes (claim 14, page 21, lines 1-2) comprises: forming sidewall spacers for the plurality of first stripes (claim 14, page 21, line 3); depositing a second material layer that covers the first stripes and fills a region between the sidewall spacers (claim 14, page 21, lines 4-5); planarizing to remove the second material layer but leave the second (claim 14, page 21, lines 6-7).

20. As to claim 26, Clementi claims that forming sidewall spacers comprises: depositing a nitride layer (claim 15, page 21, line 2); and patterning the nitride layer to remove the nitride layer above odd ones of the active areas but leave the nitride layer adjacent sidewalls of the first stripes (claim 15, page 21, lines 3-4).

Claim Rejections - 35 USC § 112

21. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

22. Claim 14 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The language "completing the formation of the floating gates by leaving the definition of the distance between floating gate regions to the spacers" is unclear and may be subject to multiple interpretations. This language could include a wide variety of semiconductor processing steps such as planarizing the surface, depositing additional layers, or selective removal by etching.

Claim Rejections - 35 USC § 103

23. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

24. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of

35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

25. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kerber, in view of Kim et al. (U.S. Patent No. 5,510,286).

26. As to claim 1, Kerber discloses a method for manufacturing non-volatile memory cells on a semiconductive substrate, comprising at least the following steps: forming active areas (column 6, lines 12-15; column 1, lines 28-35) in said semiconductive substrate (100), bounded by portions of an insulating layer (20) (column 6, lines 24-25; Figure 2A); forming a first thin layer of tunnel oxide (30) (column 6, line 26) and depositing a first layer of conductive material (50) on said active areas (column 6, lines 27-29).

27. Kerber does not expressly disclose defining a plurality of floating gate regions, including the seven elements claimed by the Applicants. Kerber teaches that a floating gate structures require opening with small dimensions (column 6, lines 8-15). Kim, as a general teaching reference, discloses a method, including forming a plurality of alternated stripes (4) of a first material above active alternated by areas lacking stripes (column 2, lines 31-33, Figure 1A); forming spacers (5) of a second material in the shelter of the side walls of said stripes (4) (column 2, lines 37-40; Figure 1A), said second material being selectively etchable with respect to said first material (column 2, lines 48-50), depositing a layer of a third material (6) in order to fill in the space between said spacers (column 2, lines 40-45; Figure 1B), planarizing said layer of a third material together with said alternated stripes (4/6) and said spacers (5) (column 2, lines

40-45), selectively removing said spacers (5) in order to expose portions of said first layer of semiconductive material (3) (column 2, lines 48-50; Figures 1B-1C), etching said first layer of semiconductive material (3) in order to form grooves in correspondence with its exposed portions (column 2, lines 51-52; Figure 1C), selectively removing said alternated stripes (4) and said layer of a third material (6) (column 2, lines 52-53). Kim's method produces contact holes for a semiconductor device in which the resolution is close to the resolution limit of photoresist film patterns (column 1, lines 50-54). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to define a plurality of floating gate regions, wherein the definition of the floating gate regions comprises the steps of: forming a plurality of alternated stripes of a first material above active areas alternated by active areas lacking stripes; forming spacers of a second material in the shelter of the side walls of said stripes, said second material being selectively etchable with respect to said first material, depositing a layer of a third material in order to fill in the space between said spacers, planarizing said layer of a third material together with said alternated stripes and said spacers, selectively removing said spacers in order to expose portions of said first layer of semiconductive material, etching said first layer of semiconductive material in order to form grooves in correspondence with its exposed portions, selectively removing said alternated stripes and said layer of a third material. One who is skilled in the art would be motivated use a method that increases the resolution for the formation of contact holes.

28. Claims 2-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kerber, in view of Kim, in further view of Wolf et al., *Silicon Processing for the VLSI Era*, Vol. 1, Lattice Press (1986).

29. As to claim 2, Kerber does not expressly disclose that said first material and said third material are a conductive material. Wolf teaches that thin film polysilicon has many important applications as a conductor in integrated circuit technology, including compatibility with high temperature processing, an excellent interface with silicon oxide and conformity over steep topography (page 175). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form said first material and said third material of a conductive polysilicon material. One who is skilled in the art would be motivated to use a common semiconductor conductor material with beneficial properties, known to be compatible with semiconductor processing.

30. As to claim 3, Kim discloses that said plurality of alternated stripes (4) is formed by depositing a second layer of material and by defining said second layer of material by means of lithography (column 2, lines 30-31; Figure 1A).

31. As to claim 4, Kerber do not expressly disclose that between said first layer of semiconductive material and said second layer of semiconductive material a thin oxide layer is interposed. Wolf teaches that silicon oxide is widely used in semiconductor processing and is used as insulating layers, diffusion and implantation masks, capping layers, and passivation layers (pages 182-183). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to interpose between said first layer of

semiconductive material and said second layer of semiconductive material a thin oxide layer. One who is skilled in the art would be motivated to use a common insulating material with beneficial properties, known to be compatible with semiconductor processing.

32. As to claim 5, Kim discloses that formation of said spacers (5) in the shelter of the side walls of said alternated stripes (4) comprises the deposition of an insulating layer, which is patterned by means of an anisotropic etching (column 2, lines 37-40; Figure 1B). Kim does not expressly disclose that said insulating layer is silicon nitride. Wolf teaches that silicon nitride is a widely used insulating material used in semiconductor fabrication, including as passivation and mechanical protection, as an oxidation mask, and as a gate dielectric (page 191). Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to use silicon nitride as in insulating layer. One who is skilled in the art would be motivated to use a common insulating material with beneficial properties, known to be compatible with semiconductor processing.

33. As to claim 6, Kim does not expressly disclose that said first material and said third material are each an oxide. Wolf teaches that silicon oxide is widely used in semiconductor processing and is used as insulating layers, diffusion and implantation masks, capping layers, and passivation layers (pages 182-183). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form said first material and said third material each of oxide. One who is skilled in the art would be motivated to use a common

insulating material with beneficial properties, known to be compatible with semiconductor processing.

34. As to claim 7, Kim discloses that said plurality of alternated stripes (4) is formed by depositing a first layer and by defining said first layer by means of lithography (column 2, lines 31-32). See also, Wolf, pages 407-408.

35. As to claim 8, Kim discloses that formation of said spacers (5) in the shelter of the side walls of said alternated stripes (4) comprises the deposition of an insulating layer, which is patterned by means of an anisotropic etching (column 2, lines 37-40; Figure 1B). Kim does not expressly disclose that said insulating layer is silicon nitride. Wolf teaches that silicon nitride is a widely used insulating material used in semiconductor fabrication, including as passivation and mechanical protection, as an oxidation mask, and as a gate dielectric (page 191). Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to use silicon nitride as in insulating layer. One who is skilled in the art would be motivated to use a common insulating material with beneficial properties, known to be compatible with semiconductor processing.

36. Claims 9, 13-14, and 30-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kerber (U.S. Patent No. 6,027,972).

37. As to claim 9, Kerber discloses a method for manufacturing non-volatile memory cells on a semiconductive substrate, comprising at least the following steps: forming active areas (column 6, lines; column 1, lines 28-35) in said semiconductive substrate (100), bounded by portions of an insulating layer (20) (column 6, lines 24-25; Figure 2A); forming a first thin tunnel oxide layer (30)

(column 6, line 26) and depositing a first layer of conductive material (50) on said active areas (column 6, lines 27-29); defining a plurality of floating gate regions, wherein the definition of the floating gate regions comprises the steps of: forming a plurality of stripes (60) of a first material above active areas (column 6, lines 28-30); forming spacers (70) of a second material in the shelter of the side walls of said alternated stripes (60) (column 6, lines 30-34; Figure 2A), said second material being selectively etchable with respect to said first material (column 6, lines 35-39; Figure 2B), selectively removing said plurality of alternated stripes (60) (column 6, lines 35-39; Figure 2B), depositing a layer of a third material (80) between said spacers (70) (column 6, lines 35-38), selectively removing said spacers (70) in order to expose portions of said first layer of semiconductive material (50) (column 6, lines 38-41; Figure 2C), etching said first layer of semiconductive material (80) in order to form grooves in correspondence of its exposed portions (column 6, lines 38-41; Figure 2C), selectively removing said layer of a third material (80) (column 6, lines 42-43). Although Kerber discloses the processing of a single device, during semiconductor processing, a plurality of devices are inherently fabricated. See Streetman, *Solid State Electronic Devices*, Prentice Hall (1990), page 332.

38. Kerber does not expressly disclose forming a plurality of alternated stripes of a first material above active areas alternated by active areas lacking stripes. However, Kerber teaches forming a spacer above a region which is subjected to a selective etch to produce a small line-type structure (column 3, lines 55-67; column 4, lines 1-4). Kerber further teaches using the method to form small

structures in MOS transistors and memory cells (column 4, lines 36-42). Thus, one who is skilled in the art would alter the dimensions and spacing of first material (60), to accurately place the sidewall (70) over a desirable location with respect to the underlying semiconductor structure. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a plurality of alternated stripes of a first material above active areas alternated by active areas lacking stripes. One who is skilled in the art would be motivated to accurately place the sidewall over a desirable location with respect to the underlying semiconductor structure.

39. As to claim 13, Kerber discloses that said second material (70) is silicon nitride and wherein the formation of said spacers in the shelter of side walls of said alternated stripes comprises the deposition of a silicon nitride layer, which is patterned by means of anisotropic etching (column 6, lines 30-34; Figure 2A).

40. As to claim 14, Kerber discloses a method for manufacturing non-volatile memory cells on a semiconductor substrate, comprising: forming active areas (column 6, lines 12-15; column 1, lines 28-35) in said semiconductor substrate (100), bounded by portions of an insulating layer (20) (column 6, lines 24-25; Figure 2A); depositing a first thin layer of tunnel oxide (30) (column 6, line 26) and a first layer of conductive material (50) on said active areas (column 6, lines 27-29); and defining a plurality of floating gate regions, comprising: forming stripes (60) of shielding material (column 6, lines 28-30); defining spacers (70) of small width in the shelter of the side walls of the stripes (60) thus defined (column 6, lines 30-34; Figure 2A); and completing the formation of the floating gates by

leaving the definition of the distance between floating gate regions to the spacers (column 6, lines 35-59). Although Kerber discloses the processing of a single device, during semiconductor processing, a plurality of devices are inherently fabricated. See Streetman, page 332.

41. Kerber does not expressly disclose forming stripes of shielding material only above pairs of alternated active areas; and defining stripes of shielding material also on the active areas that lacked them. However, Kerber teaches forming a spacer above a region which is subjected to a selective etch to produce a small line-type structure (column 3, lines 55-67; column 4, lines 1-4). Kerber further teaches using the method to form small structures in MOS transistors and memory cells (column 4, lines 36-42). Thus, one who is skilled in the art would alter the dimensions and spacing of first material (60), to accurately place the sidewall (70) over a desirable location with respect to the underlying semiconductor structure. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to forming stripes of shielding material only above pairs of alternated active areas; and defining stripes of shielding material also on the active areas that lacked them. One who is skilled in the art would be motivated to accurately place the sidewall over a desirable location with respect to the underlying semiconductor structure.

42. As to claim 30, Kerber discloses a semiconductor fabrication method, comprising: forming a plurality of stripes (60) over an insulated base polysilicon layer (50) (column 6, lines 23-28); forming sidewall spacers (70) for the plurality of stripes (column 6, lines 30-34; Figure 2A); removing the stripes (60) but

leaving the sidewall spacers (70) (column 6, lines 35-39; Figure 2B); forming an oxide layer (80) over the insulated base polysilicon layer (50) between the sidewall spacers (column 6, lines 35-38); and removing the sidewall spacers (70) (column 6, lines 38-41; Figure 2C). Although Kerber discloses the processing of a single device, during semiconductor processing, a plurality of devices are inherently fabricated. See Streetman, page 332.

43. Kerber does not expressly disclose forming a plurality of stripes which lie above first alternating active areas. However, Kerber teaches forming a spacer above a region which is subjected to a selective etch to produce a small line-type structure (column 3, lines 55-67; column 4, lines 1-4). Kerber further teaches using the method to form small structures in MOS transistors and memory cells (column 4, lines 36-42). Thus, one who is skilled in the art would alter the dimensions and spacing of first material (60), to accurately place the sidewall (70) over a desirable location with respect to the underlying semiconductor structure. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a plurality of stripes which lie above first alternating active areas. One who is skilled in the art would be motivated to accurately place the sidewall over a desirable location with respect to the underlying semiconductor structure.

44. As to claim 31, Kerber discloses that forming the plurality of stripes (60) with conventional photolithography (column 6, lines 29-30). Conventional photolithography inherently comprises: depositing a material layer; defining the stripes in the material layer using a photolithography mask; etching using the

mask to remove the material layer but leave the stripes. See Wolf, pages 407-408.

45. As to claim 32, Kerber discloses that forming sidewall spacers comprises: depositing a nitride layer; and patterning the nitride layer to remove the nitride layer above second alternating active areas but leave the nitride layer adjacent sidewalls of the stripes (column 6, lines 30-34; Figure 2A).

46. As to claim 33, Kerber discloses using the oxide layer (80) between the removed spacers as a hard mask (column 6, lines 38-41; Figure 2C); and etching using the oxide layer hard mask to define floating gate regions in the base polysilicon layer (column 6, lines 50-54; Figure 2E).

47. Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kerber, in view of Wolf.

48. As to claim 10, Kerber discloses that said third material (80) is an oxide being thermally grown (column 6, lines 38-41). Kerber does not expressly disclose that that said first material (60) is a conductive material. Wolf teaches that thin film polysilicon has many important applications as a conductor in integrated circuit technology, including compatibility with high temperature processing, an excellent interface with silicon oxide and conformity over steep topography (page 175). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the first material of a conductive polysilicon material. One who is skilled in the art would be motivated to use a common semiconductor conductor material with beneficial properties, known to be compatible with semiconductor processing.

49. As to claim 11, Kerber discloses that said plurality of alternated stripes (50) is formed by depositing a second layer of material and by defining said second layer of material by means of lithography (column 6, lines 28-30).

50. As to claim 12, Kerber does not expressly disclose that between said first layer of conductive material and said second layer of conductive material a thin oxide layer is interposed. Wolf teaches that silicon oxide is widely used in semiconductor processing and is used as insulating layers, diffusion and implantation masks, capping layers, and passivation layers (pages 182-183). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to interpose between said first layer of conductive material and said second layer of conductive material a thin oxide layer. One who is skilled in the art would be motivated to use a common insulating material with beneficial properties, known to be compatible with semiconductor processing.

51. Claims 15-17, 19, 22-25, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim, in view of Kerber.

52. As to claim 15, Kim discloses a semiconductor fabrication method, comprising, forming a plurality of first stripes (4) which lie above first alternating active areas (column 2, lines 31-33, Figure 1A); forming sidewall spacers (5) for the plurality of first stripes (4) (column 2, lines 37-40; Figure 1B); forming a plurality of second stripes (6) between the sidewall spacers which lie above second alternating active areas (column 2, lines 40-45; Figure 1B); and removing the sidewall spacers (5) (column 2, lines 48-50; Figures 1B-1C).

53. Kim does not expressly disclose an insulated base polysilicon layer. However, Kim discloses that the semiconductor substrate may include isolation films, gate electrodes, and source electrodes (column 2, lines 25-29). Kerber teaches that an insulated base polysilicon layer (50) (column 6, lines 23-28) is conventional structure in memory cells (column 6, lines 12-15). Therefore, it would have been obvious to one of ordinary skill in the art to form a plurality of first stripes over an insulated base polysilicon layer. One who is skilled in the art would be motivated to use a conventional structure in forming a memory device.

54. As to claim 16, Kim discloses that forming the plurality of first stripes comprises: depositing photoresist film patterns (4) (column 2, lines 30-31; Figure 1A). This step inherently includes depositing a first material layer; defining the first stripes in the first material layer using a photolithography mask; etching using the mask to remove the first material layer but leave the first stripes. See Wolf, pages 407-408.

55. As to claim 17, Kim discloses that forming the plurality of second stripes comprises: depositing a second material layer that covers the first stripes (4) and fills a region between sidewall spacers (5) (column 2, lines 40-44; Figure 1B); planarizing to remove the second material layer but leave the second stripes (column 2, lines 40-44; Figure 1B).

56. As to claim 19, Kim discloses using the first (4) and second stripes (6) as a hard mask (column 2, lines 48-50); and etching using the first and second stripes hard mask (column 2, lines 50-51). Kim does not expressly disclose etching to define floating gate regions in the base polysilicon layer above both

the first and second alternating active areas. However, Kim's method produces contact holes for a semiconductor device in which the resolution is close to the resolution limit of photoresist film patterns (column 1, lines 50-54). Kerber teaches that a floating gate structures also require opening with small dimensions (column 6, lines 8-15). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to etch to define floating gate regions in the base polysilicon layer above both the first and second alternating active areas. One who is skilled in the art would be motivated use a method that increases the resolution for the formation of contact holes.

57. As to claim 22, Kim discloses a method for semiconductor fabrication on a substrate including a plurality of active areas, comprising: forming a plurality of first stripes (4) by photolithographic techniques (column 2, lines 31-33) which lie above even ones of the plurality of active areas (Figure 1B); and forming a plurality of second stripes (6) without the use of photolithographic techniques which lie above odd ones of the plurality of active areas (column 2, lines 40-44).

58. Kim does not expressly disclose an insulated base polysilicon layer. However, Kim discloses that the semiconductor substrate may include isolation films, gate electrodes, and source electrodes (column 2, lines 25-29). Kerber teaches that an insulated base polysilicon layer (50) (column 6, lines 23-28) is conventional structure in memory cells (column 6, lines 12-15). Therefore, it would have been obvious to one of ordinary skill in the art to form a plurality of first stripes over an insulated base polysilicon layer. One who is skilled in the art would be motivated to use a conventional structure in forming a memory device.

59. As to claim 23, Kim discloses that forming the plurality of first stripes comprises: depositing photoresist film patterns (4) (column 2, lines 30-31; Figure 1A). This step inherently includes depositing a first material layer; defining the first stripes in the first material layer using a photolithography mask; etching using the mask to remove the first material layer but leave the first stripes. See also Wolf, pages 407-408.

60. As to claim 24, Kim discloses forming the plurality of second stripes comprises: forming sidewall spacers (5) for the plurality of first stripes (4) (column 2, lines 37-40); forming the plurality of second stripes (6) between the sidewall spacers over odd ones of the active areas (column 2, lines 40-45); and removing the sidewall spacers (column 2, lines 48-50; Figure 1C).

61. As to claim 25, Kim discloses forming the plurality of second stripes comprises: forming sidewall spacers (5) for the plurality of first stripes (4) (column 2, lines 37-40); depositing a second material layer (6) that covers the first stripes and fills a region between the sidewall spacers (5) (column 2, lines 40-44); planarizing to remove the second material layer but leave the second (column 2, lines 40-44).

62. As to claim 27, Kim discloses using the first (4) and second stripes (6) as a hard mask (column 2, lines 48-50); and etching using the first and second stripes hard mask (column 2, lines 50-51). Kim does not expressly disclose etching to define floating gate regions in the base polysilicon layer above both the odd and even ones of the active areas. However, Kim's method produces contact holes for a semiconductor device in which the resolution is close to the

resolution limit of photoresist film patterns (column 1, lines 50-54). Kerber teaches that a floating gate structures also require opening with small dimensions (column 6, lines 8-15). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to etch to define floating gate regions in the base polysilicon layer above both the odd and even ones of the active areas. One who is skilled in the art would be motivated use a method that increases the resolution for the formation of contact holes.

63. Claims 18, 20-21, 26, and 28-29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim, in view of Kerber, in further view of Wolf.

64. As to claims 18, Kim discloses forming sidewall spacers comprises: depositing an insulating layer (5); and patterning the insulating layer to remove the insulating layer above the second alternating active areas but leave the insulating layer adjacent sidewalls (5) of the first stripes (4) (column 2, lines 37-40).

65. Kim does not expressly disclose that the insulating layer is nitride. Wolf teaches that silicon nitride is a widely used insulating material used in semiconductor fabrication, including as passivation and mechanical protection, as an oxidation mask, and as a gate dielectric (page 191). Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to use nitride as in insulating layer. One who is skilled in the art would be motivated to use a common insulating material with beneficial properties, known to be compatible with semiconductor processing.

66. As to claims 20 and 28, Kim does not expressly disclose that the first and second stripes are formed from polysilicon material. Wolf teaches that thin film polysilicon has many important applications in integrated circuit technology, including compatibility with high temperature processing, an excellent interface with silicon oxide and conformity over steep topography (page 175). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to the form the first and second stripes from polysilicon material. One who is skilled in the art would be motivated to use a common semiconductor material with beneficial properties, known to be compatible with semiconductor processing.

67. As to claim 21 and 29, Kim does not expressly disclose that the first and second stripes are formed from oxide material. Wolf teaches that silicon oxide is widely used in semiconductor processing and is used as insulating layers, diffusion and implantation masks, capping layers, and passivation layers (pages 182-183). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the first and second stripes from oxide material. One who is skilled in the art would be motivated to use a common insulating material with beneficial properties, known to be compatible with semiconductor processing.

68. As to claims 26, Kim discloses forming sidewall spacers comprises: depositing an insulating layer (5); and patterning the insulating layer to remove the insulating layer above odd ones of the active areas but leave the insulating layer adjacent sidewalls (5) of the first stripes (4) (column 2, lines 37-40).

69. Kim does not expressly disclose that the insulating layer is nitride. Wolf teaches that silicon nitride is a widely used insulating material used in semiconductor fabrication, including as passivation and mechanical protection, as an oxidation mask, and as a gate dielectric (page 191). Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to use nitride as in insulating layer. One who is skilled in the art would be motivated to use a common insulating material with beneficial properties, known to be compatible with semiconductor processing.

Conclusion

70. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Hsue (U.S. Patent No. 5,310,693) discloses a method of patterning a polysilicon layer using silicon nitride sidewall spacers. Huang (U.S. Patent No. 5,998,287) discloses using silicon nitride vertical sidewalls as masking stripes. Bergemont (U.S. Patent No. 5,688,705) discloses forming features beyond the resolution of photolithography by incorporating sacrificial sidewall spacers. Daemen et al. (U.S. Patent No. 6,624,027) discloses using a nitride sidewall as a mask to form a tunnel oxide window.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric B. Chen whose telephone number is (571) 272-2947. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine G. Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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EBC EBC
Aug. 15, 2005

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